REMARKS

This is a preliminary amendment to a continued prosecution application, mailed on January 3, 2003, of U.S. Application Serial No. 09/475,717. Claims 1, 3-6, 8-12, and 14-27 are currently pending for examination. Claims 2, 7, and 13 are canceled herein without prejudice. Claims 1, 3, 4, 8, 10, 14, 15, and 17 are amended herein. Claims 18-27 are newly presented. Entry of this preliminary amendment and consideration of claims 1, 3-6, 8-12, and 14-27 are respectfully requested.

Drawings

In an Office Action mailed September 3, 2002, the Examiner objected to the drawings filed with the original application. Responsive to this objection, Applicants are submitting formalized drawings.

Claim Rejections – 35 U.S.C. §102

Claims 1-17 were rejected in the Office Action mailed September 3, 2002 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,363,515 B1 to Rajgopal et al. ("Rajgopal"). Claims 1-17 were further rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,798,938 to Heikes et al ("Heikes").

A claim is anticipated only if each and every element of the claim is found in a single reference. M.P.E.P § 2131 (citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628 (Fed. Cir. 1987)). "The identical invention must be shown in as complete detail as is contained in the claim." M.P.E.P. § 2131 (citing *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226 (Fed. Cir. 1989)).

Amended independent claim 1 now recites in pertinent part, "each domino logic circuit simulated after any domino logic circuit feeding into at least one of the inputs of the domino logic circuit has been simulated...." Applicants submit that Rajgopal fails to disclose simulating a domino logic circuit after any domino logic circuit feeding into its inputs has been simulated. Rajgopal is directed towards "a method of estimating power use by a proposed electronic system design before the design is completed..." Rajgopal col. 2, lines 15-17. In particular, Rajgopal discloses:

> The input activity factor of blocks downstream from a domino block is changed as a result of the upstream domino blocks. The *logic simulator does not correct these downstream blocks* for the effect of the upstream use of domino blocks. Therefore, the AF values of the downstream blocks may be corrected at block 68 to account for the effect of the upstream domino blocks.

Rajgopal col. 4, lines 14-21 (Emphasis added). Thus, Rajgopal discloses a simulator that does not correct downstream blocks for the effect of the upstream use of domino blocks. Applicant's claimed invention addresses this simulation problem by simulating each domino logic circuit after any domino logic circuit feeding into a domino logic circuit has been simulated. Rajgopal fails to disclose ordering the simulation of domino logic circuits as claimed by claim 1.

Heikes also fails to anticipate amended claim 1. In particular, Heikes is directed towards "a system and method for performing precharge timing verification on a logic circuit..."and "determining the longest precharge path in the logic circuit." Heikes Abstract. However, Heikes fails to disclose simulating a domino logic circuit after any domino logic circuit feeding into it has been simulated. Consequently, each and every element of claim 1 is not found in Rajgopal or Heikes. Accordingly, Applicants respectfully request that the instant §102(e) rejections of claim 1 be withdrawn.

Amended independent claims 4, 10, 15, and 17 all now recite in pertinent parts, "the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list...." Furthermore, these claims recite in pertinent parts, "simulating each domino logic circuit according to the ordered list." As discussed above, Applicants submit that both Rajgopal and Heikes fail to disclose simulating an ordered list that positions all domino logic circuits feeding into another domino logic circuit before the another domino logic circuit. Accordingly, Applicants respectfully request that the instant §102(e) rejections of claims 4, 10, 15, and 17 be withdrawn.

Claim Rejections – 35 U.S.C. §103

Claim1 stands rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No.: 6,040,716 to Bosshart ("Bosshart") in view of Heikes.

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. M.P.E.P § 2143.03 (citing *In re Royka*, 490 F.2d 981).

Amended independent claim 1 now recites in pertinent part, "each domino logic circuit simulated after any domino logic circuit feeding into at least one of the inputs of the domino logic circuit has been simulated...." Neither Bosshart nor Heikes disclose, teach, or fairly suggest a method of simulating a domino logic circuit after any domino logic circuit feeding into it is simulated. Therefore, the combination of Bosshart and Heikes fail to teach or suggest each element of claim 1 as required

Applicants note that some of the limitations of cancelled claim 2 have been moved into independent claim 1. Cancelled claim 2 stood rejected by the Examiner under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No.: 5,815,687 to Masleid et al. ("Masleid") in view of Heikes and in further view of Rajgopal. In support of this rejection the Examiner stated, "the Masleid et al. reference discloses simulating each domino logic circuit after any circuits coupled to the set of inputs have been simulated..." Applicants respectfully disagree. In particular, Masleid is directed to an "apparatus for and method of testing CMOS domino logic circuits in which pre-chard validation and functional evaluation are separated." Masleid col. 3, lines 6-8. However, Masleid, Heikes and Rajgopal, either alone or in combination, fail to disclose, teach, or fairly suggest a method of simulating a domino logic circuit after any domino logic circuit feeding into it has been simulated. Accordingly, Applicants respectfully request the instant §103(a) rejection of claim 1 be withdrawn.

Claims 4-9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Bosshart in view of Heikes and in further view of Rajgopal.

Amended independent claim 4 now recites in pertinent part, "the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list...." As discussed above, Bosshart, Heikes, and Rajgopal, either alone or in combination, fail to disclose, teach, or fairly suggest an ordered list positioning all domino logic circuits feeding into another domino logic circuit before the another domino logic circuit. Consequently, Applicants respectfully request that the instant §103(a) rejection of claim 4 be withdrawn.

Claims 10-16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No.: 5,825,673 to Watanabe ("Watanabe") in view of Rajgopal.

Amended independent claims 10 and 15 recite in pertinent parts, "the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list...." The Examiner stated in the Office Action mailed September 3, 2002 that, "the Watanabe reference does not expressly disclose simulating each domino circuit, scheduling of the domino circuits in an ordered list such that all circuits coupled to an input of a first domino logic circuit are placed in the ordered list at a position in the ordered list before a position in the ordered list of the first domino circuit." As discussed above in connection with the §102(e) rejection of claim 1, Applicants submit that Rajgopal also fails to disclose, teach, or fairly suggest an ordered list positioning all domino logic circuits feeding into another domino logic circuit before the another domino logic circuit in the ordered list. Accordingly, since each element of claims 10 and 15 are not taught or suggested by the combination of Watanabe and Rajgopal, Applicants request that the instant §103(a) rejections be withdrawn.

Claim 17 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Masleid in view of Heikes and in further view of Rajgopal.

Amended independent claim 17 recites in pertinent part, "the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list...." As discussed above in connection with claim 1, the combination of Masleid, Heikes and Rajgopal fails to teach or suggest every element of amended claim 17. Accordingly, Applicants respectfully request the instant §103(a) rejection be withdrawn.

Dependent claims 3, 5, 6, 8, 9, 11, 12, 14, and 16 are patentable over the prior art of record for at least the same reasons as discussed above in connection with their respective independent claims, in addition to adding further limitations of their own. Accordingly, Applicants respectfully request that the instant §102(e) and §103 rejections for claims 3, 5, 6, 8, 9, 11, 12, 14, and 16 be withdrawn.

New Claims

New claims 18, 20, 22, 24, and 26 recite in pertinent parts, "simulating each domino logic circuit includes generating output results of each domino logic circuit, the output results including worst-case noise that will be generated by each domino logic circuit." Applicants submit that the prior art of record fails to disclose, teach, or fairly suggest generating output results including worst case noise.

New claims 19, 21, 23, 25, and 27 recite in pertinent parts, "indicating whether each domino logic circuit is likely to generate an erroneous output." Applicants submit that the prior art of record fails to disclose, teach, or fairly suggest the claimed indication. Applicants believe that dependents claims 18-27 add additional patentable subject matter to their respective independent parent claims.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants believe the applicable rejections have been overcome and all claims remaining in the application are presently in condition for allowance. Accordingly, favorable consideration and a Notice of Allowance are earnestly solicited. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

CHARGE DEPOSIT ACCOUNT

Please charge any additional fees or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

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Date: Feb. 25, 2003

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

1. (Amended) A method comprising:

extracting parameters of a set of domino logic circuits, each domino logic circuit of the set of domino logic circuits having inputs and an output;

simulating each domino logic circuit of the set of domino logic circuits, each domino logic circuit simulated after any domino logic circuit feeding into at least one of the inputs of the domino logic circuit has been simulated; and

reporting results of the simulating.

3. (Amended) The method of claim [2]1 wherein:

simulating each domino logic circuit includes using the simulated results of circuits coupled to the inputs of the domino logic circuit.

4. (Amended) A method, comprising:

scheduling a set of domino logic circuits into an ordered list, the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list; and

simulating each domino logic circuit according to the ordered list.

8. (Amended) The method of claim [7]6 wherein:

the extracting further including extracting parameters of non-domino circuits;

the scheduling further including scheduling non-domino circuits into the ordered list; and

the simulating further including simulating non-domino circuits.

10. (Amended) A machine readable medium embodying instructions which, when executed by a processor, cause the processor to perform a method, the method comprising:

scheduling a set of domino logic circuits into an ordered list, the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list; and

simulating each domino logic circuit according to the ordered list.

14. (Amended) The machine readable medium of claim [13]12 further embodying instructions which, when executed by a processor, cause the processor to perform the method wherein:

the extracting further including extracting parameters of non-domino circuits;

the scheduling further including scheduling non-domino circuits into the ordered list; and

the simulating further including simulating non-domino circuits.

15. (Amended) A system comprising:

a processor;

a memory controller coupled to the processor;

a memory coupled to the memory controller;

wherein the processor executes instructions to perform the method of:

scheduling a set of domino logic circuits into an ordered list, the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list; and

simulating each domino logic circuit according to the ordered list.

17. (Amended) An apparatus comprising:

means for extracting parameters for each domino logic circuit of a set of domino logic circuits;

means for scheduling the set of domino logic circuits into an ordered list, the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list;

means for simulating each domino logic circuit according to the ordered list

means for reporting results of the means for simulating.